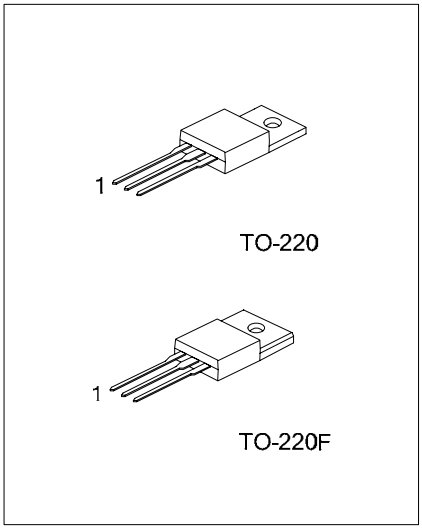
18Amps, 500 Volts N-CHANNEL MOSFET



*Pb-free plating product number:18N50

■ DESCRIPTION

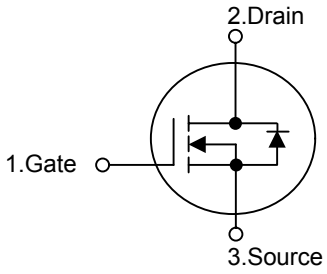
The YR18N50 are N-Channel enhancement mode power field effect transistors (MOSFET) which are produced using YR's proprietary, planar stripe, DMOS technology.

These devices are suited for high efficiency switch mode power supply. To minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode the advanced technology has been especially tailored.

■ FEATURES

* $R_{DS(ON)}$ = 0.48Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 42 nC)
* Low reverse transfer capacitance (C_{RSS} = typical 34 pF)
* Fast switching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25℃, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage	18N50	V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Avalanche Current (Note 1)		I_{AR}	18	A
Continuous Drain Current		I_D	18	A
Pulsed Drain Current (Note 1)		I_{DM}	72	A
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	330	mJ
	Repetitive (Note 1)	E_{AR}	28	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	6.9	V/ns
Junction Temperature		T_J	+150	℃
Operating Temperature		T_{OPR}	-55 ~ +150	℃
Storage Temperature		T_{STG}	-55 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_C =25℃, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	18N50	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V			10	μA
Gate-Source Leakage Current		I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Breakdown Voltage Temperature Coefficient		$\triangle BV_{DSS}/\triangle T_J$	I_D = 250 μA, Referenced to 25°C		0.7		V/℃
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS} = 10V, I_D = 9.0A			0.48	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz		1480	1900	pF
Output Capacitance		C_{OSS}			200	270	pF
Reverse Transfer Capacitance		C_{RSS}			25	35	pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D(ON)}$	V_{DD} = 400V, I_D = 18A, R_G = 25Ω (Note 4, 5)		30	70	ns
Turn-On Rise Time		t_R			115	240	ns
Turn-Off Delay Time		$t_{D(OFF)}$			95	200	ns
Turn-Off Fall Time		t_F			85	180	ns
Total Gate Charge		Q_G	V_{DS}= 400V,I_D= 18A, V_{GS}= 10 V (Note 4, 5)		42	54	nC
Gate-Source Charge		Q_{GS}			8.6		nC
Gate-Drain Charge		Q_{GD}			21		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS} = 0 V, I_S = 18A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current		I_S				18	A
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}				72	A
Reverse Recovery Time		t_{RR}	V_{GS} = 0 V, I_S = 18A, dI_F/dt = 100 A/μs (Note 4)		520		ns
Reverse Recovery Charge		Q_{RR}			5.3		μC

Notes:1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 10mH, I_{AS} = 18A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 18A, di/dt ≤200A/s, V_{DD} ≤BV_{DSS} Starting T_J = 25°C
4. Pulse Test : Pulse width ≤300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

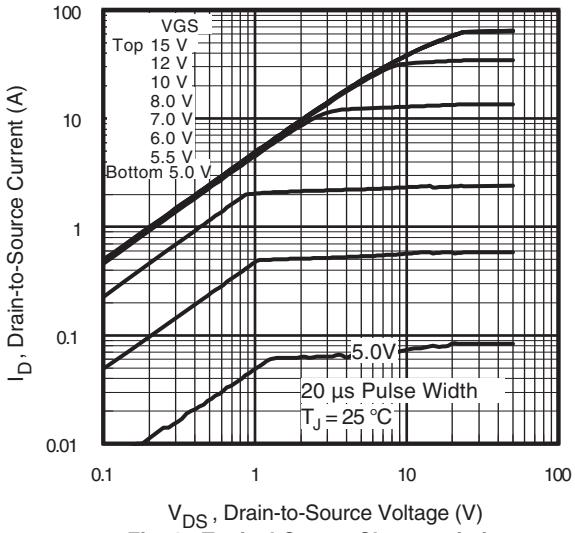


Fig. 1 - Typical Output Characteristics

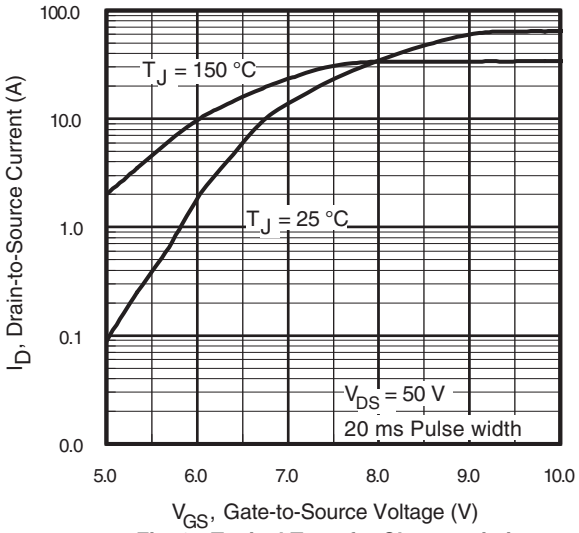


Fig. 3 - Typical Transfer Characteristics

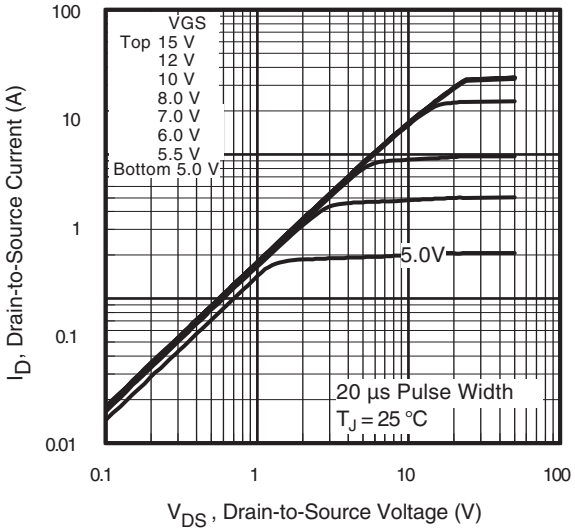


Fig. 2 - Typical Output Characteristics

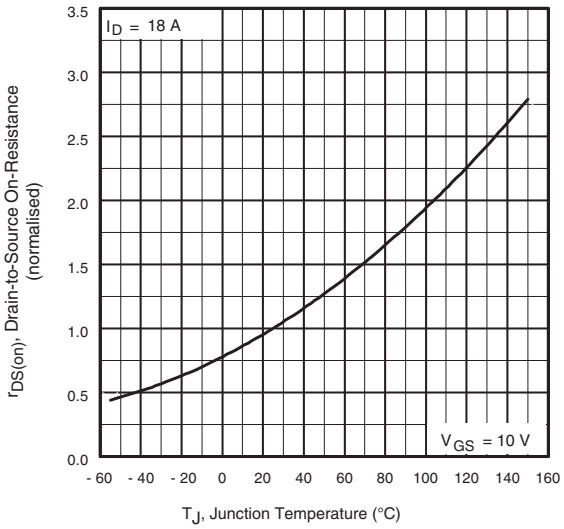


Fig. 4 - Normalized On-Resistance vs. Temperature

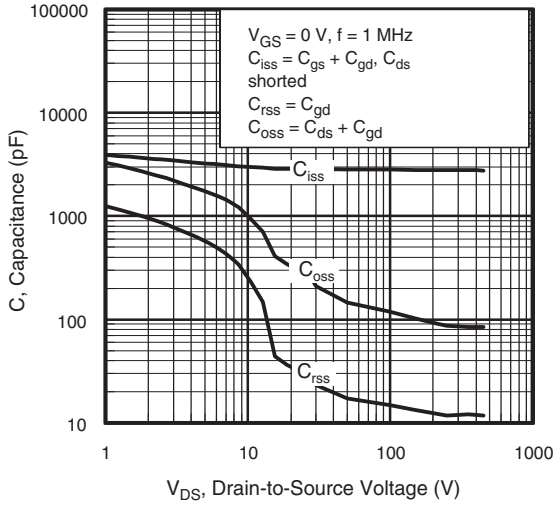


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

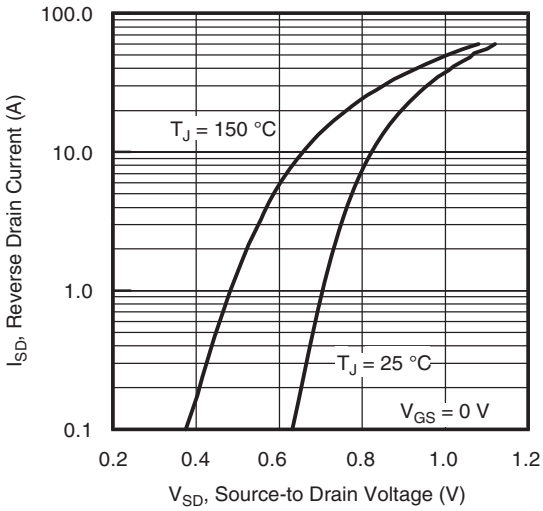


Fig. 7 - Typical Source-Drain Diode Forward Voltage

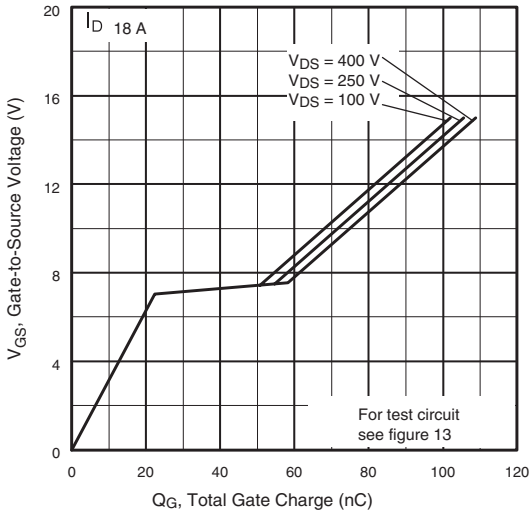


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

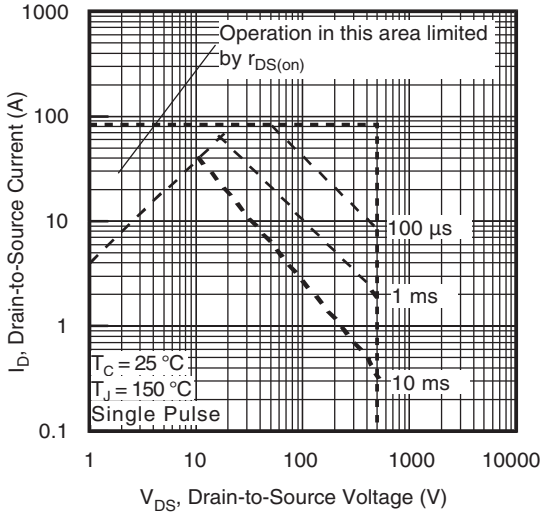


Fig. 8 - Maximum Safe Operating Area

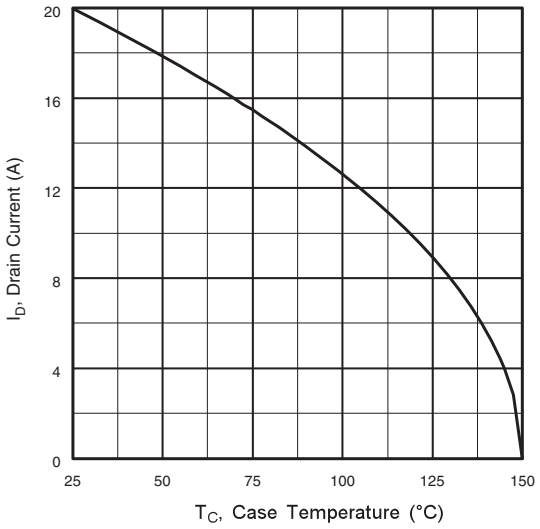


Fig. 9 - Maximum Drain Current vs. Case Temperature

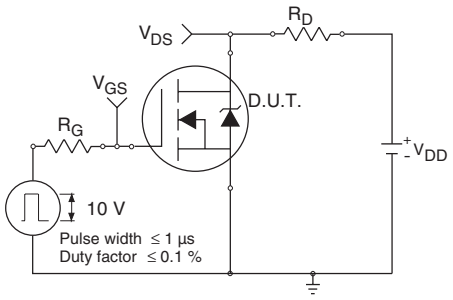


Fig. 10a - Switching Time Test Circuit

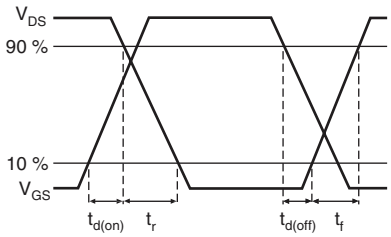


Fig. 10b - Switching Time Waveforms

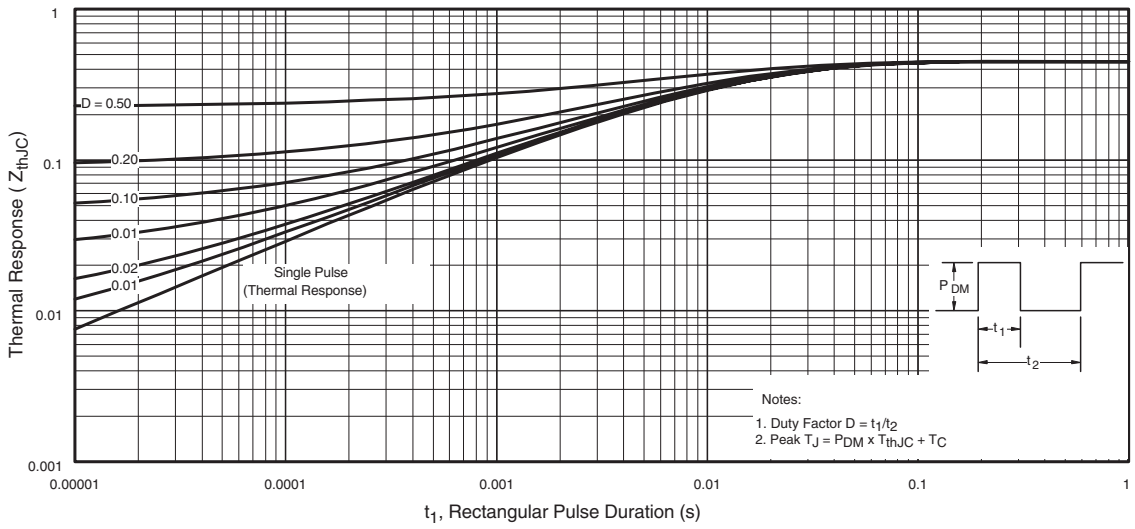


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

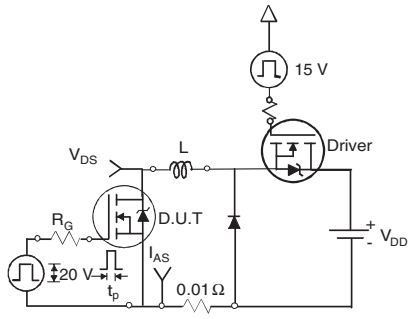


Fig. 12a - Unclamped Inductive Test Circuit

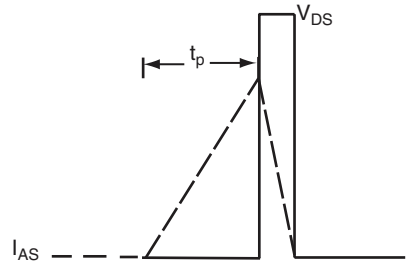


Fig. 12b - Unclamped Inductive Waveforms

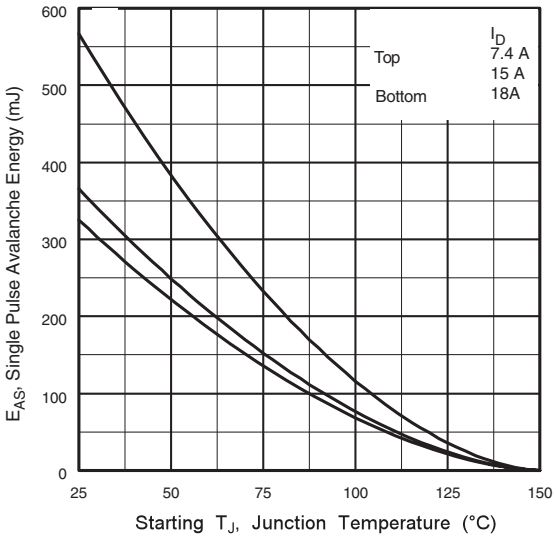


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

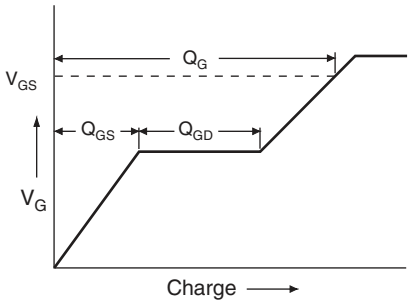


Fig. 13a - Basic Gate Charge Waveform

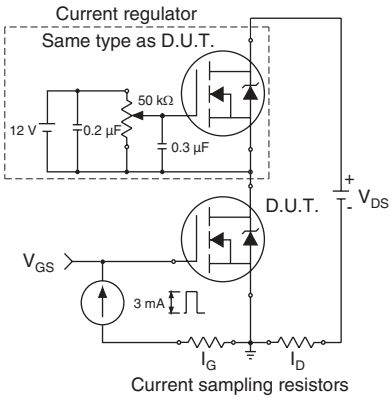
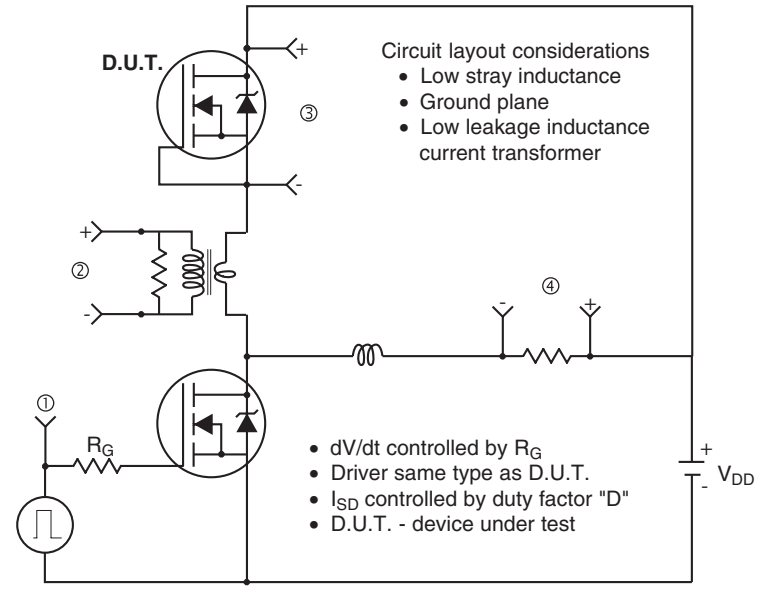
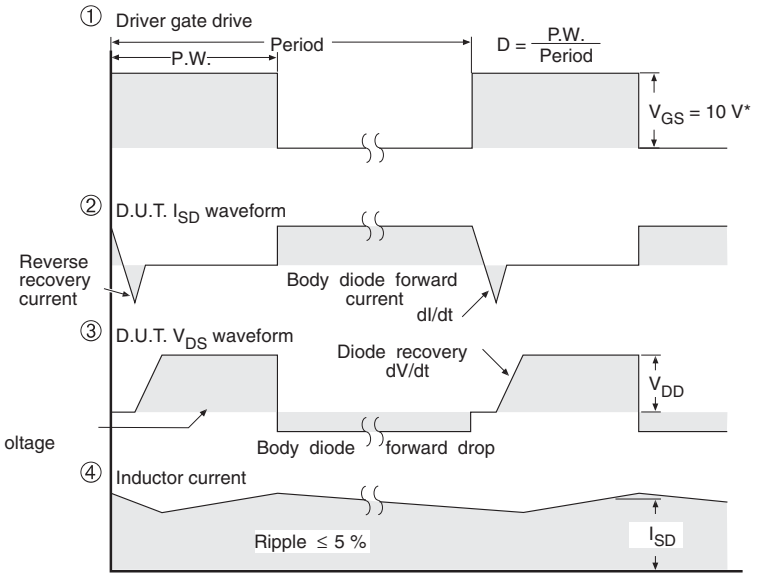


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel